Listing of Claims

1. (Currently Amended) A semiconductor device, comprising:

a first layer having a plurality of signal wires; and

a second layer adjacent to the first layer having a plurality of signal wires, wherein the signal wires in the first ~~and second layers~~ layer are substantially parallel with ~~each other~~ the signal wires in the second layer and wherein adjacent signal wires are located in an alternating pattern in the first and second layers.

2. (Canceled)

3. (Currently Amended) The semiconductor device of claim 1 [[2]], wherein the alternating pattern has every other signal wire residing in the same layer.

4. (Original) The semiconductor device of claim 1, wherein power supply and ground wires are located in both the first layer and the second layer.

5. (Original) The semiconductor device of claim 4, wherein power supply and ground wires are located in the same respective position in each layer.

6. (Canceled)

7. (Currently Amended) A [[The]] semiconductor device ~~of claim 6~~, comprising:

a first layer having a plurality of signal wires;

a second layer adjacent to the first layer having a plurality of signal wires, wherein the signal wires in the first layer are substantially parallel with the signal wires in the second layer; and

at least one additional layer adjacent to the first and second layer, wherein signal wires in the at least one additional layer are substantially parallel to signal wires in the first and second layers and wherein adjacent signal wires are located in an alternating pattern in the first, second, and at least one additional layer.

8. (Original) The semiconductor device of claim 1, further comprising:

N layers, wherein N is greater than two and wherein the first and second layers are any two adjacent layers in the N layers.

9. (Original) The semiconductor device of claim 1, wherein the semiconductor device is a microprocessor.

10. (Original) The semiconductor device of claim 1, wherein the first layer and second layer have similar process parameters.

11. (Currently Amended) The semiconductor device of claim 1 [[2]], wherein the pluralities of signal wires in the first and second layer are a first set of signal wires configured to carry a first set of related signals.

12. (Original) The semiconductor device of claim 11, further comprising:

a second set of signal wires that are replicated in the first and second layers.

13. (Original) The semiconductor device of claim 1, further comprising:

additional signal wires in the second layer that are located substantially orthogonal to the plurality of signal wires in the first layer.

14. (Original) The semiconductor device of claim 1, wherein the plurality of signal wires in the first layer is a set of related signal wires and wherein the plurality of signal wires in the second layer is a replication of the plurality of signal wires in the first layer.

15-28 (Canceled)

29. (Currently Amended) A system comprising:

a microprocessor; and

an off-die component in communication with the microprocessor; wherein the microprocessor comprises:

a first layer having a plurality of signal wires; and

a second layer adjacent to the first layer having a plurality of signal wires, wherein the signal wires in the first ~~and second layers~~ layer are substantially parallel with ~~each other~~ the signal wires in the second layer and wherein adjacent signal wires are located in an alternating pattern in the first and second layers.

30. (Original) The microprocessor of claim 29, further comprising:

at least one additional layer adjacent to the first and second layers, wherein signal wires in the at least one additional layer are substantially parallel to signal wires in the first and second layers.